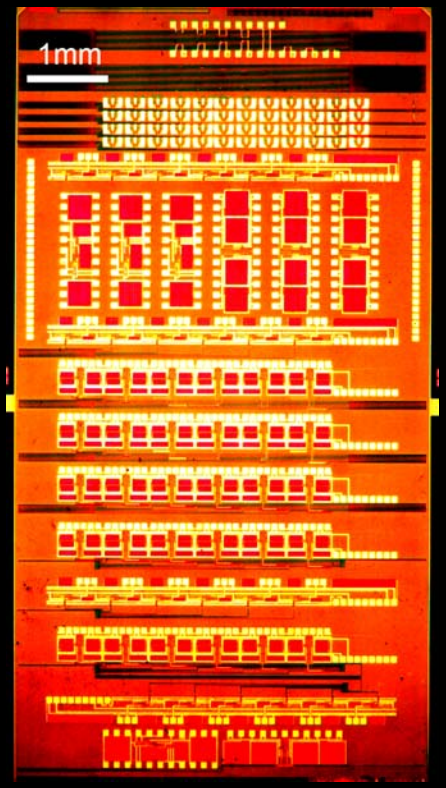
Invited talk at SEMICON 2010, December 1, Tokyo

CMOS Integrated Silicon Nanophotonics: Enabling Technology for Exascale Computational Systems



William Green
Solomon Assefa
Alexander Rylyakov
Clint Schow
Folkert Horst
Yurii Vlasov

Dr. Yurii A. Vlasov, Manager, Silicon Integrated Nanophotonics
IBM TJ Watson Research Center, Yorktown Heights, NY

Optical Interconnects in HPCS

- IBM Petascale & Exascale Computing

Building Blue Waters

Target :10PF

Blue Waters will be the most powerful computer in the world for scientific research (tentatively scheduled for Summer of 2011)

Blue Waters
~1 PF sustained
>300,000 cores
>1 PB of memory
>10 PB of disk storage
~500 PB of archival storage
>100 Gbps connectivity

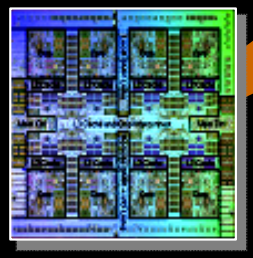
Blue Waters Building Block
32 IH server nodes
32 TB memory
256 TF (peak)
4 Storage systems
10 Tape drive connections

IH Server Node
8 MCM's (256 cores)
1 TB memory
8 TF (peak)

Fully water cooled

Multi-chip Module
4 Power7 chips
128 GB memory
512 GB/s memory bandwidth
1 TF (peak)

Router
1,128 GB/s bandwidth



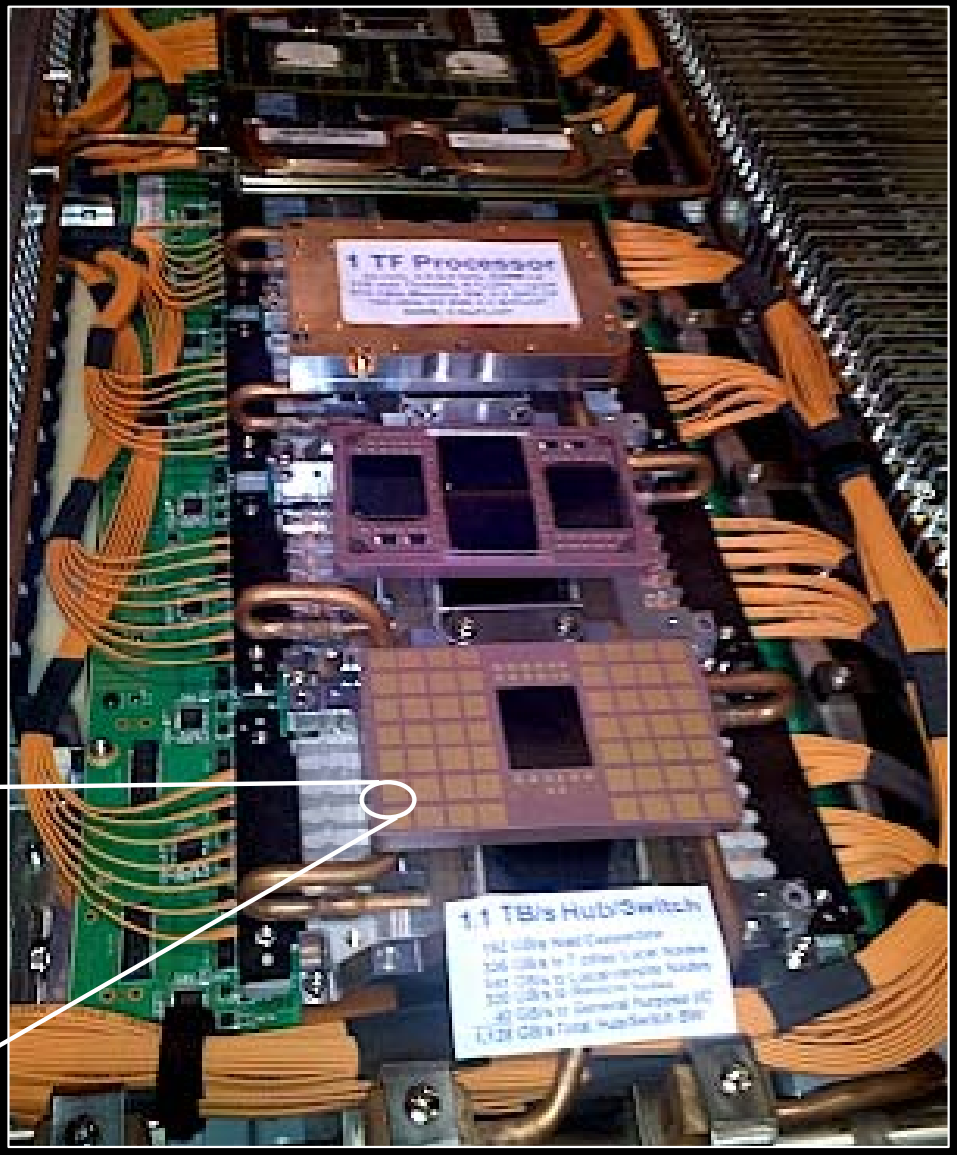
Power7 Chip
8 cores, 32 threads
L-cache (32 MB)
Up to 256 GF (peak)
45 nm technology

- Approximately 10 PF/s peak
- More than 300,000 cores (homogeneous)
- More than 1 PetaByte memory
- More than 10 Petabyte disk storage
- More than 0.5 Exabyte archival storage
- More than 1 PF/s sustained on scientific applications

Courtesy of Thomas Dunning http://www.ncsa.illinois.edu/BlueWaters

Optical Interconnect: 1.1 TB/s HUB; 1,000,000 links

- 192 GB/s Host Connection
- 336 GB/s to 7 other local nodes in the same drawer
- 240 GB/s to local-remote nodes in the same supernode (4 drawers)
- 320 GB/s to remote nodes
- 40 GB/s to general purpose I/O



Avago microPOD™

[M. Fields, Avago, OFC 2010, paper OTuP1]

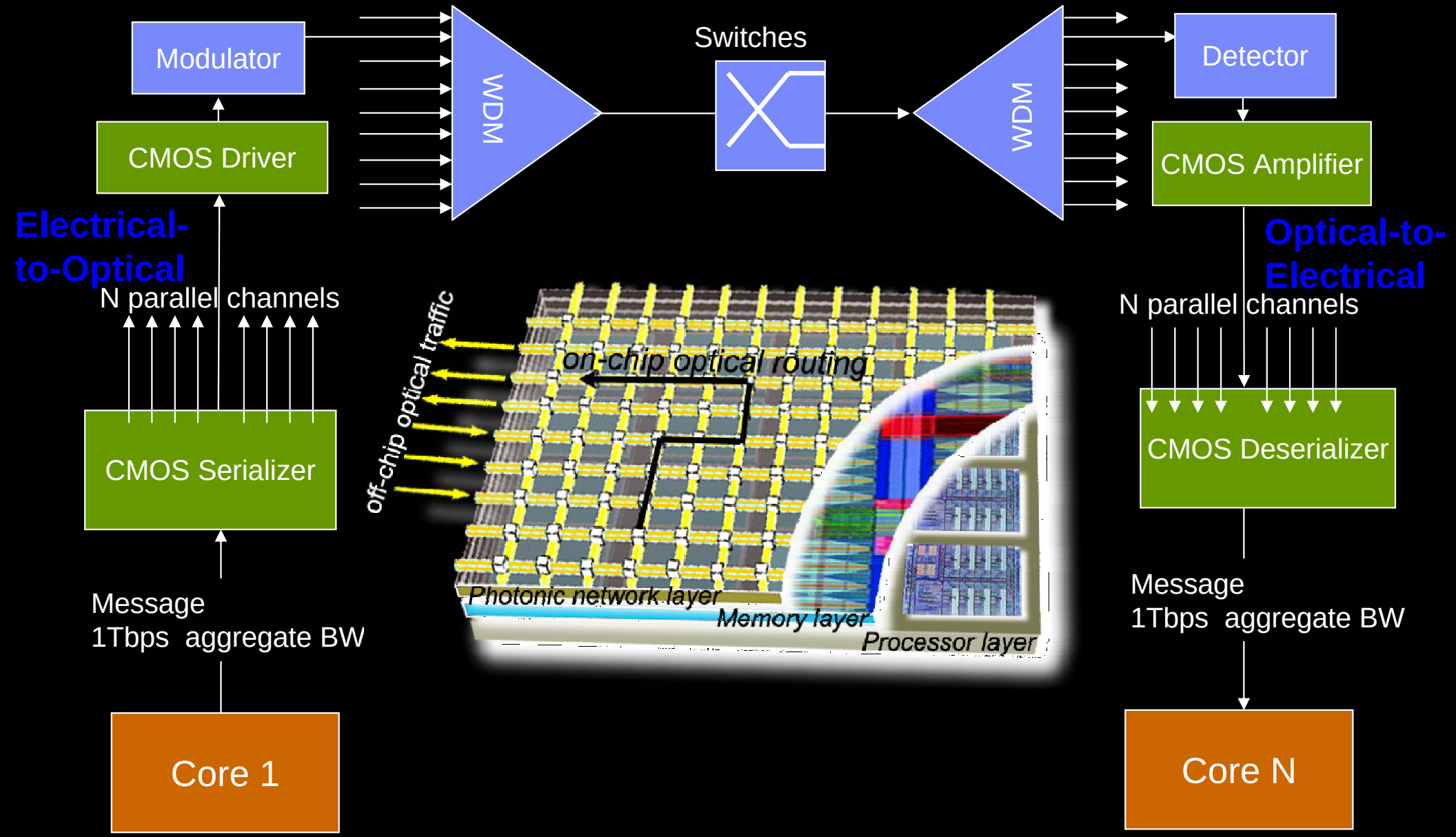
[A. Benner, IBM, OFC 2010, paper OTuH1]

http://www.ncsa.illinois.edu/BlueWaters/

Silicon Integrated Nanophotonics

- An Introduction

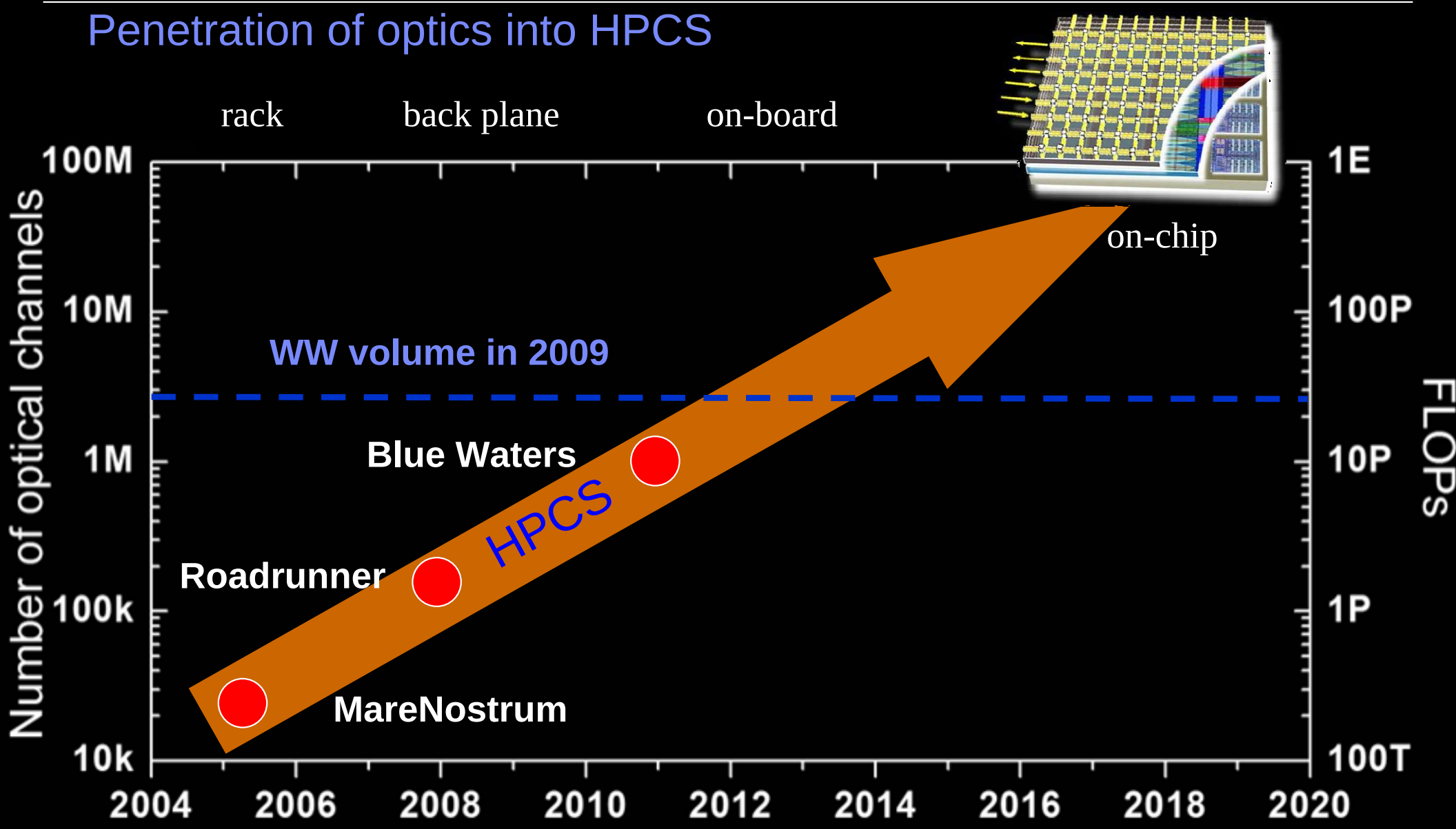
Off-Chip and On-Chip Nanophotonics Interconnects



Goal: Integrate Ultra-dense Nanophotonics Circuits with CMOS chip

http://www.research.ibm.com/photonics

Penetration of optics into HPCS

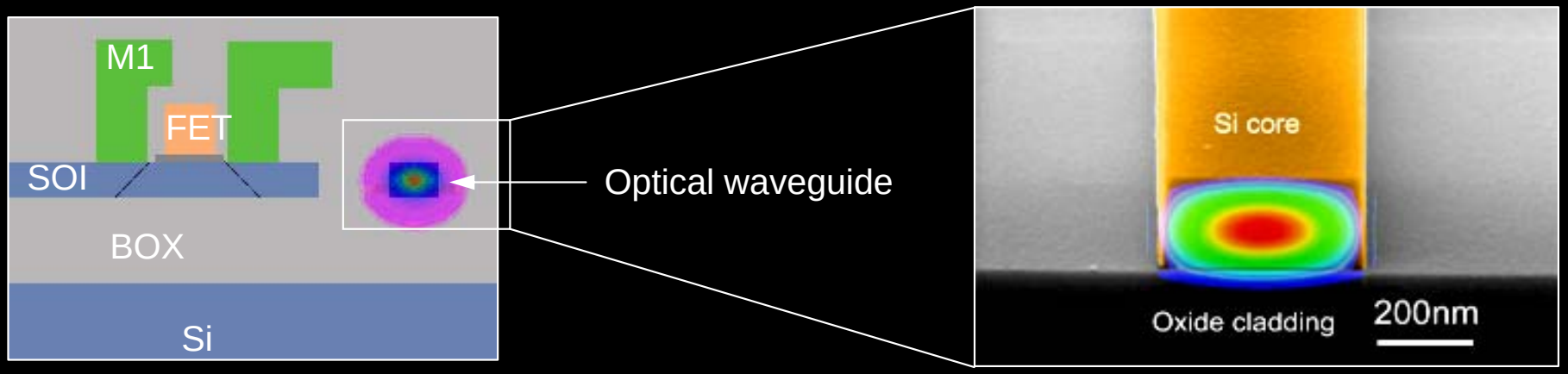


Single HPC machine will contain a similar number of optical channels as currently exist today in all parallel optical links worldwide

Courtesy of M. Taubenblatt

http://www.research.ibm.com/photonics

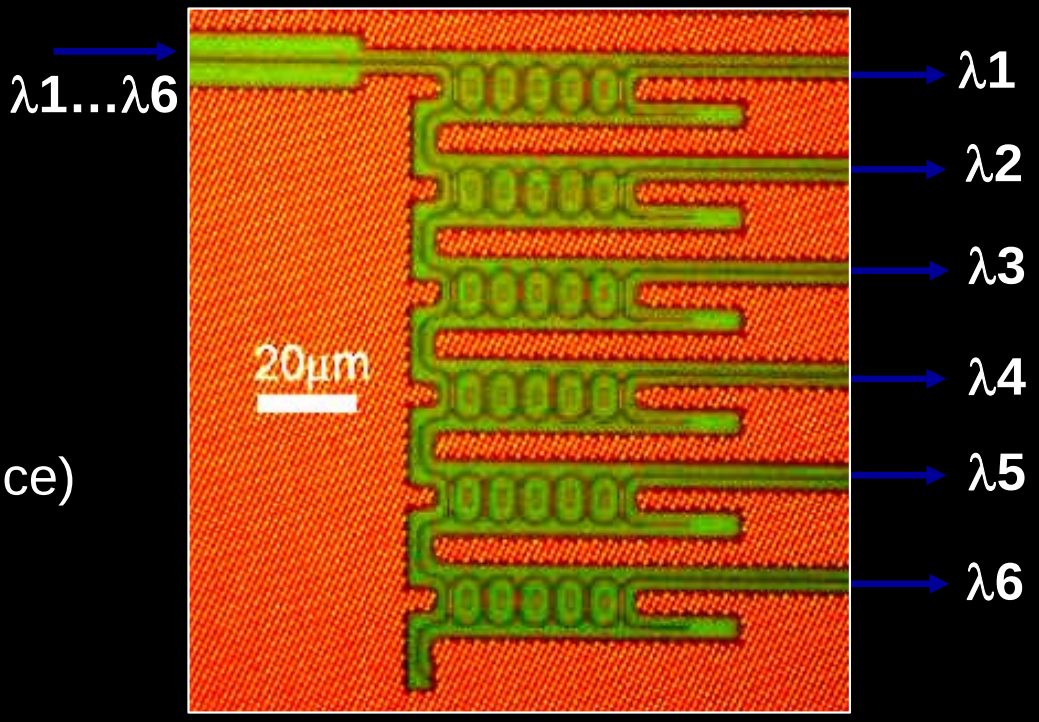
CMOS front-end monolithic Nanophotonics integration



→ Nanophotonics sharing Si layer with FET body

Advantages:

- ✓ Deeply scaled Nanophotonics
- ✓ Most dense integration with CMOS
- ✓ Ultra-low power optical interconnects
- ✓ Same mask set, standard processing
- ✓ Same design environment (e.g. Cadence)
- ✓ Same EDA tools and design flow
- ✓ Possible in-line system-level testing



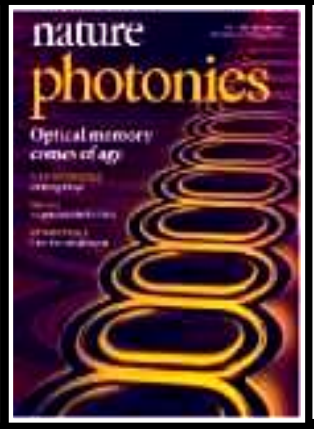
6-channel WDM

http://www.research.ibm.com/photonics

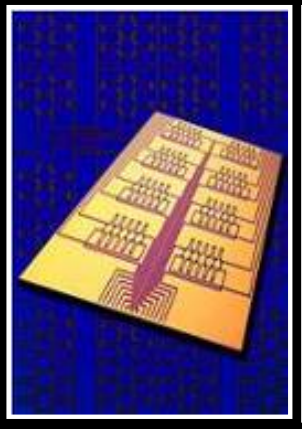
IBM Silicon Nanophotonics – Scientific Impact (2003-2010)

2005
Slow Light

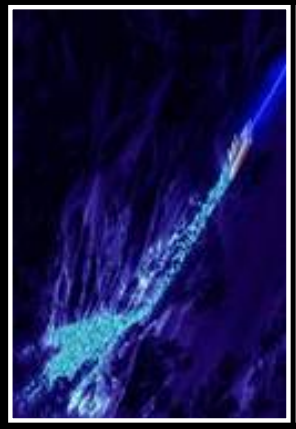
2006
Si Modulator



2007
Optical Buffer



2008
Si Switch



2009
APD Detector

2010
Amplifier

2010
Ge Receiver

Journal papers:	**>50**	**(including 5 Nature, 6 Invited)**
Conferences:	**>150**	**(including 76 Invited/Plenary)**
Citation index:	**>2,100**	
Patents:	**>30**	

World-class scientific work laid solid foundation for novel technology development

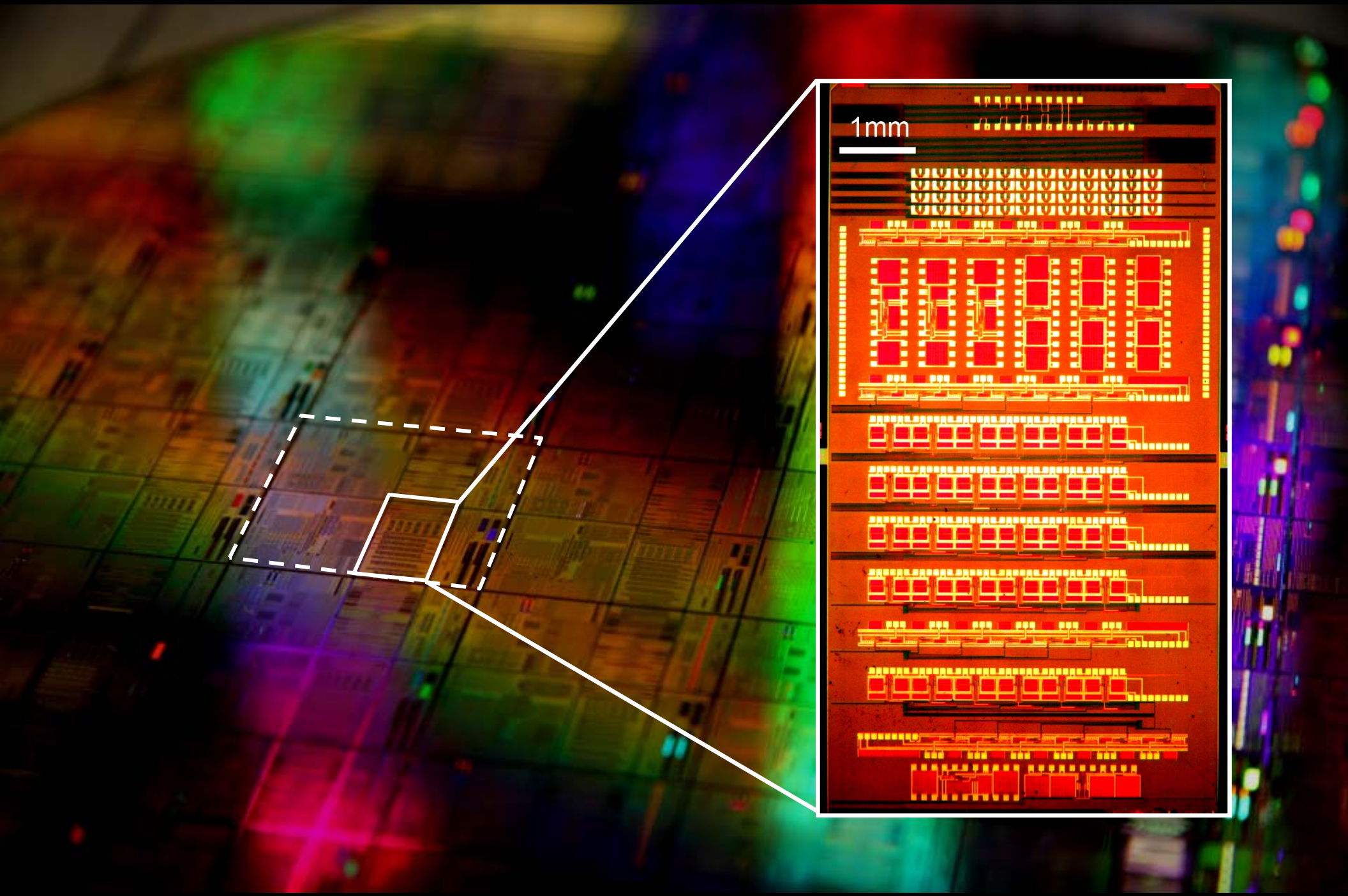
http://www.research.ibm.com/photonics

Silicon Integrated Nanophotonics

- SNIPER project at IBM Research

(Silicon Nanoscale-Integrated Photonic and Electronic tRansceiver)

IBM SNIPER Technology (2008)

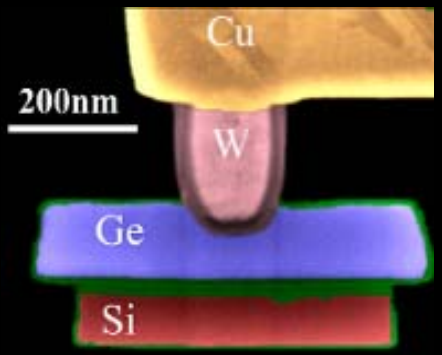


http://www.research.ibm.com/photonics

IBM SNIPER Technology (2008)

Goal: Nanophotonics devices integrated into CMOS FEOL process
(with minimal change to CMOS flow and minimal additional masks)

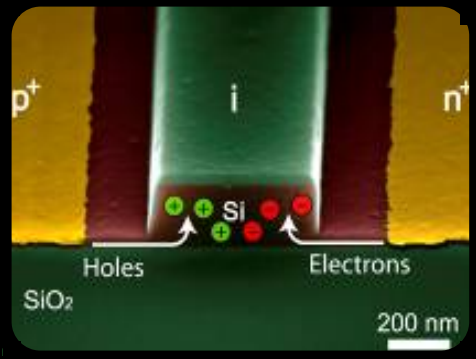
DETECTOR



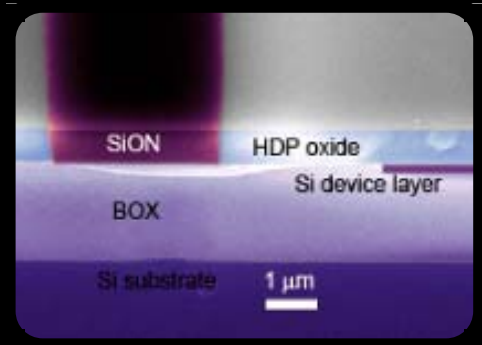
FEOL CMOS FLOW

- Shallow Trench Isolation
- Well implants/Activation
- Gate formation
- Source/Drain Activation
- Silicidation
- Cu back-end wiring

MODULATOR



FIBER COUPLER



✓Most of the mask levels and processing modules are shared

✓Minimal additional photonics modules added

Over 30 base patents

Photonics as a new feature in standard CMOS

http://www.research.ibm.com/photonics

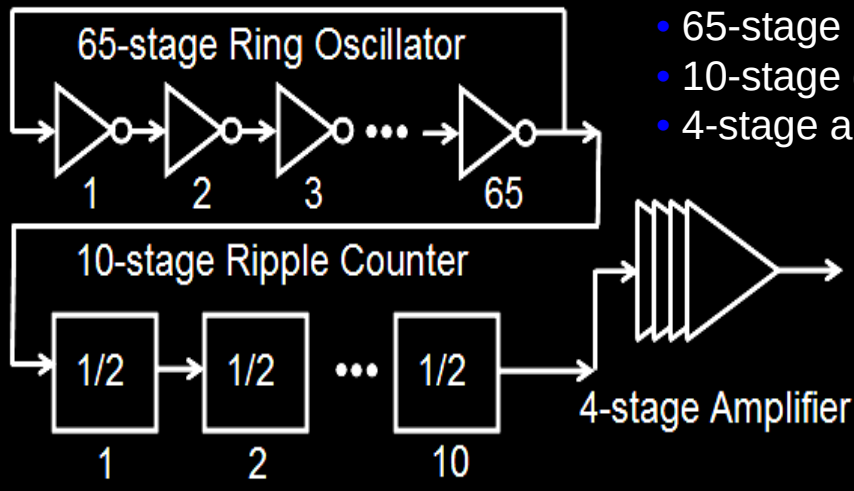
SNIPER project at IBM Research

- CMOS Transceiver components
  (after integration of all Nanophotonics modules)

CMOS performance: Digital circuits

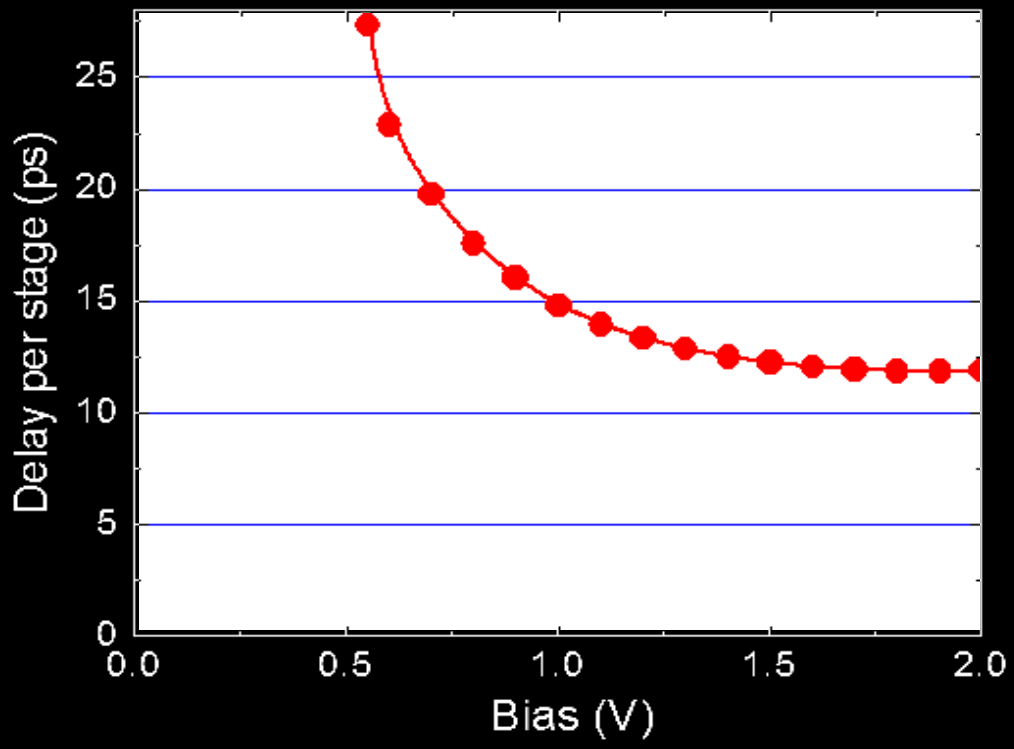
CMOS Ring Oscillator in 130nm CMOS GR

Design

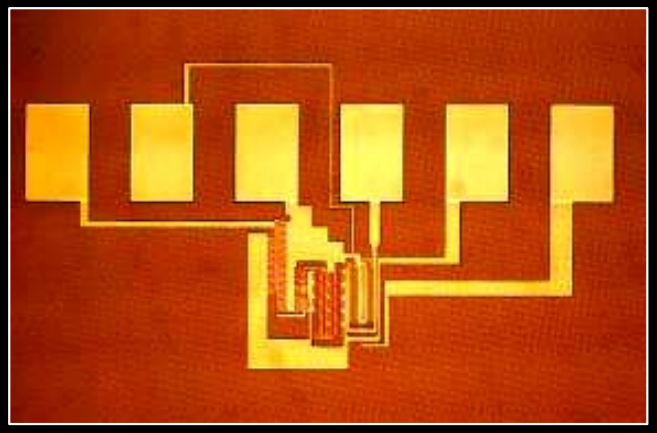


- 65-stage RO
- 10-stage divider
- 4-stage amplifier

Performance



Die photo



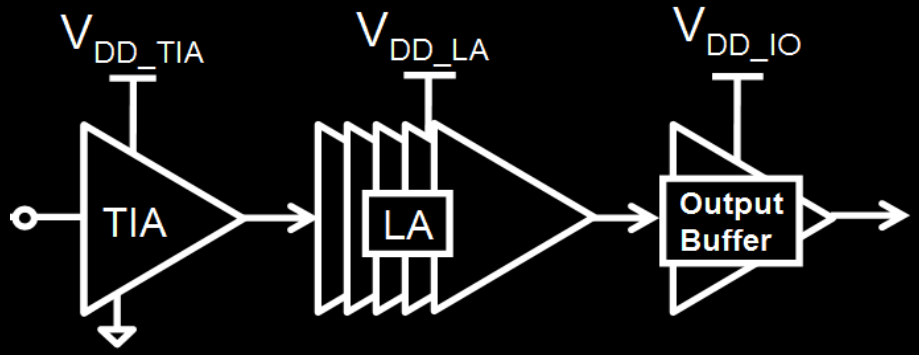
- ✓Digital CMOS Circuitry integrated with Photonics modules
- ✓130nm design rules
- ✓Ring oscillator with 12ps delay per stage

CMOS performance: Analog circuits

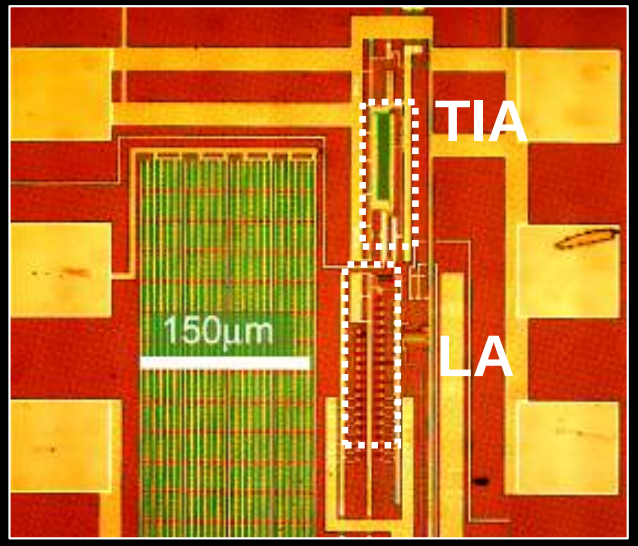
Receiver amplifier

Design

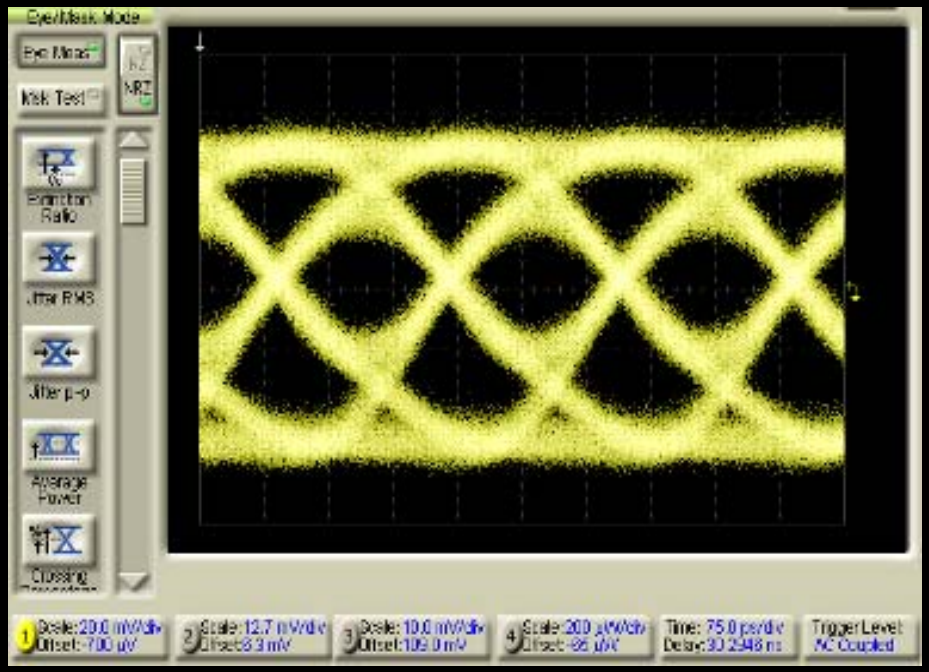
- DC-coupled common gate TIA
- 7-stage limiting amplifier LA
- open-drain output buffer.



Die photo



Performance



5Gbps open eye

- ✓Analog CMOS Circuitry integrated with Photonics modules
- ✓130nm design rules
- ✓Core area 170x40µm (TIA) and 160x50µm (LA)
- ✓28mW power consumption at 5Gbps (TIA and LA)

[Assefa et al, JSTQE, September 2010]

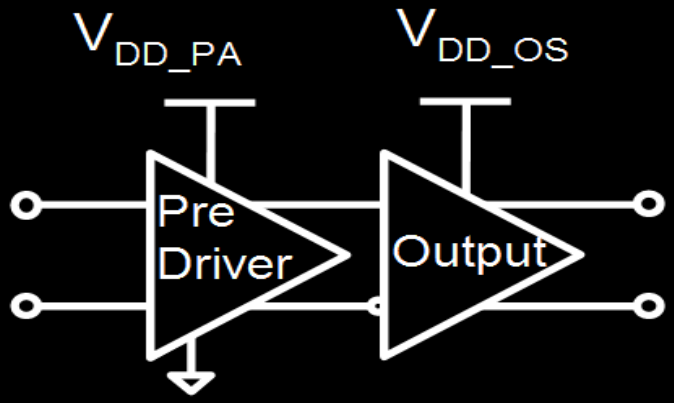
http://www.research.ibm.com/photonics

CMOS performance: Analog circuits

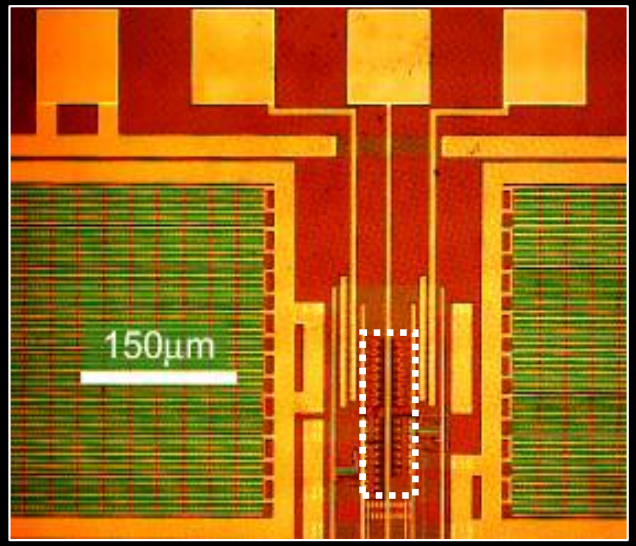
Transmitter modulator driver

Design

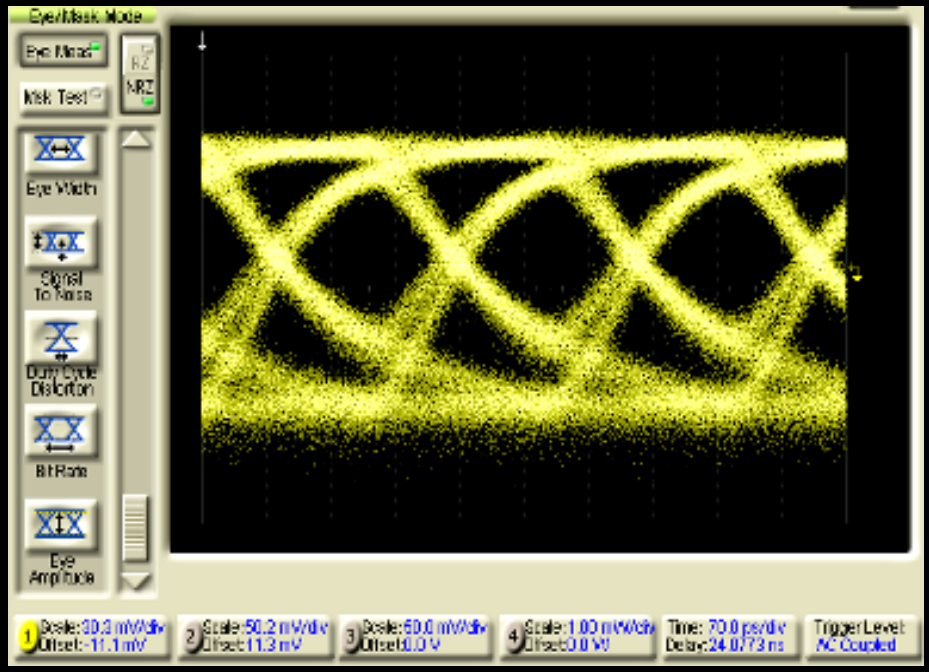
- pre-driver
- differential output buffer



Die photo



Performance



5Gbps open eye

- ✓Analog CMOS Circuitry integrated with Photonics modules
- ✓130nm design rules
- ✓Core area 170x60µm
- ✓36mW power consumption at 5Gbps

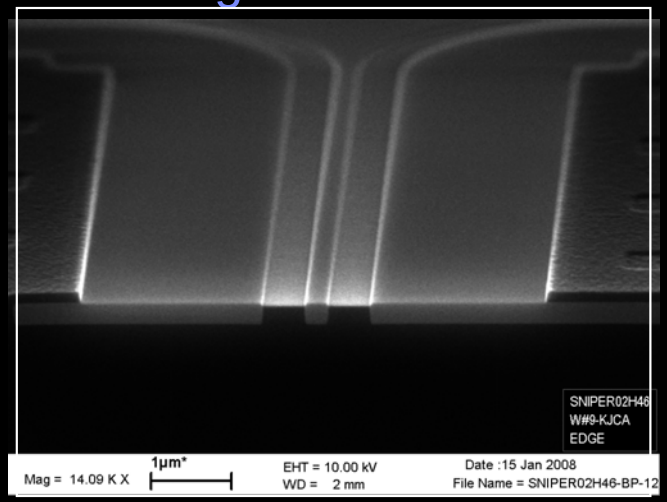
http://www.research.ibm.com/photonics

SNIPER project at IBM Research

- Nanophotonics Transceiver components

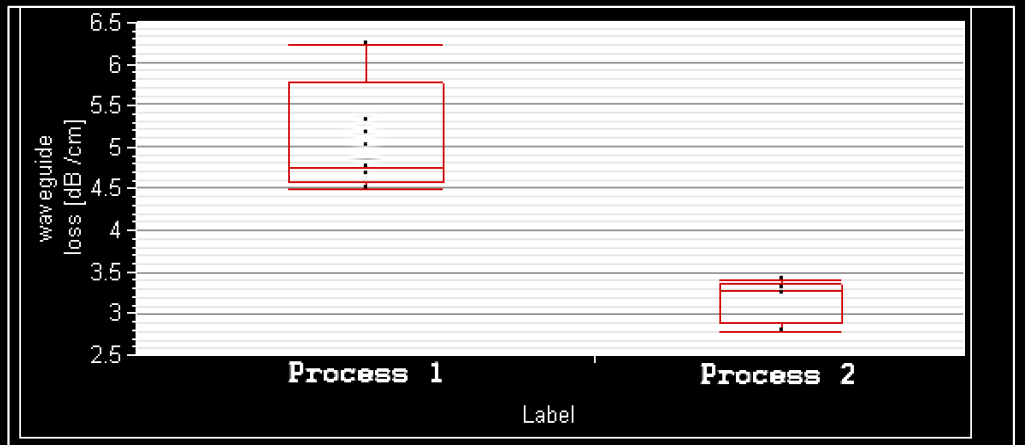
Nanophotonics components: Waveguides

Design



- ✓Formed in a standard STI process
- ✓No additional masks required
- ✓Ultra-high optical confinement (mode x-section 0.1µm^2)

Performance

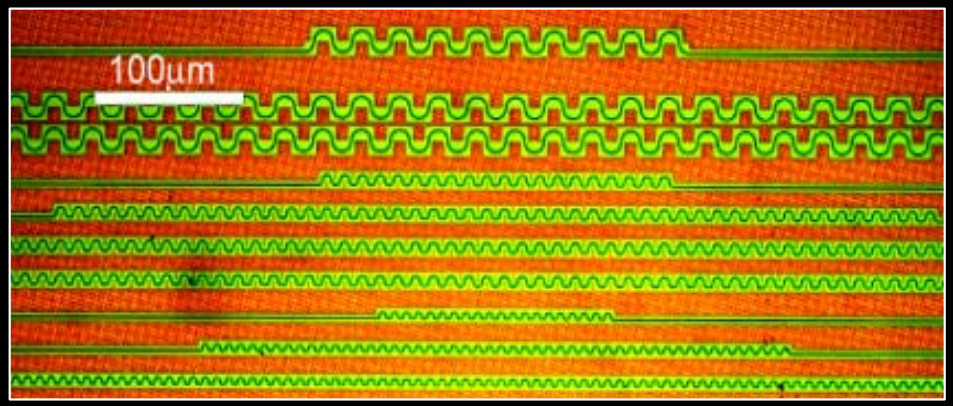


Missing Rows 1

Quantiles

Level	Minimum	10%	25%	Median	75%	90%	Maximum
Process 1	4.5	4.5	4.575	4.75	5.75	6.2	6.2
Process 2	2.8	2.8	2.9125	3.275	3.375	3.4	3.4

Die photo



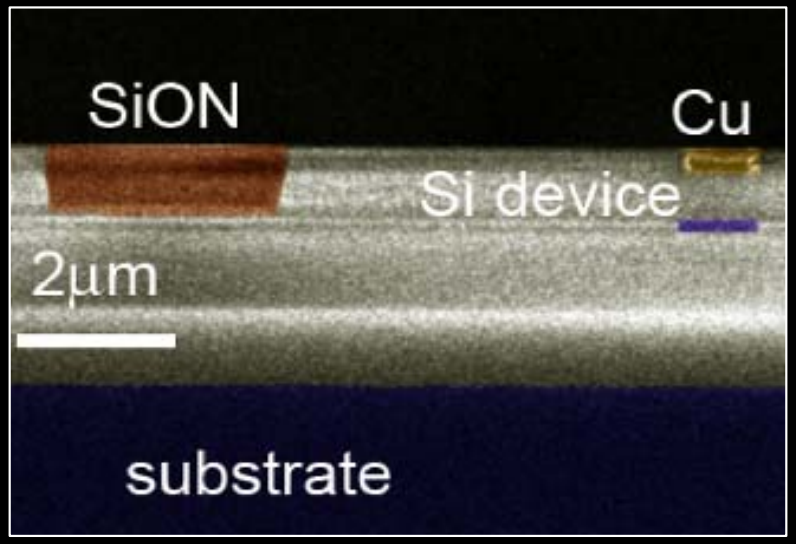
- ✓Sharp bends as small as 2µm radius

- ✓ Waveguides integrated with CMOS Circuitry
- ✓ 193nm lithography with 65nm design rules
- ✓ Bend loss 0.02dB/turn with µm-size bends
- ✓ <3dB/cm loss
- ✓ 20µm pitch between waveguides

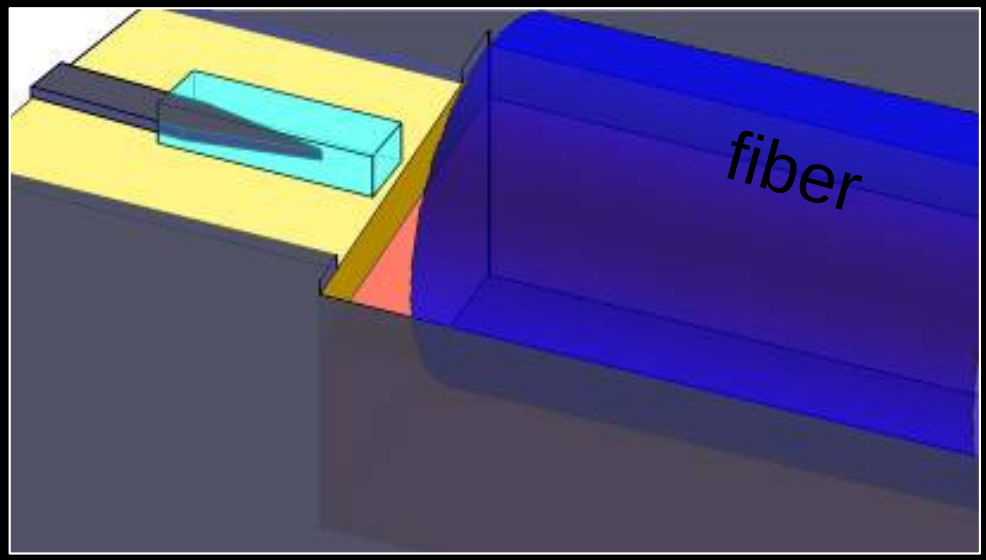
http://www.research.ibm.com/photonics

Nanophotonics components: Edge fiber coupler

Design

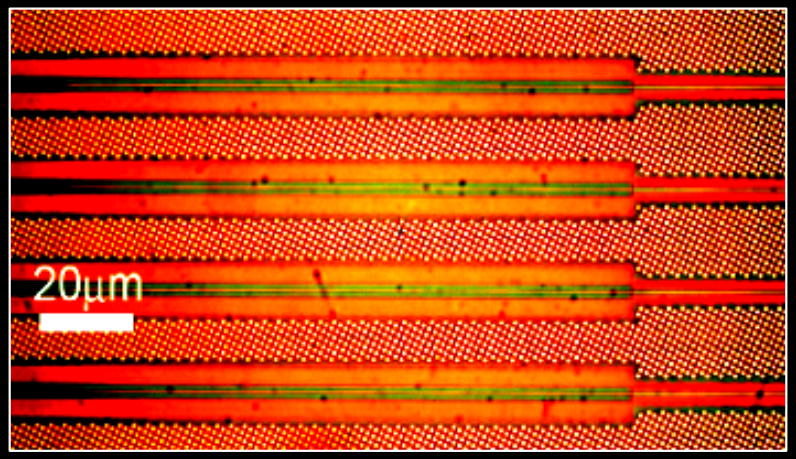


Packaging approach



8Tbps per 1mm of chip edge

Die photo



- ✓ Coupler arrays integrated with CMOS Circuitry
- ✓ 20um pitch
- ✓ Coupling loss <1dB

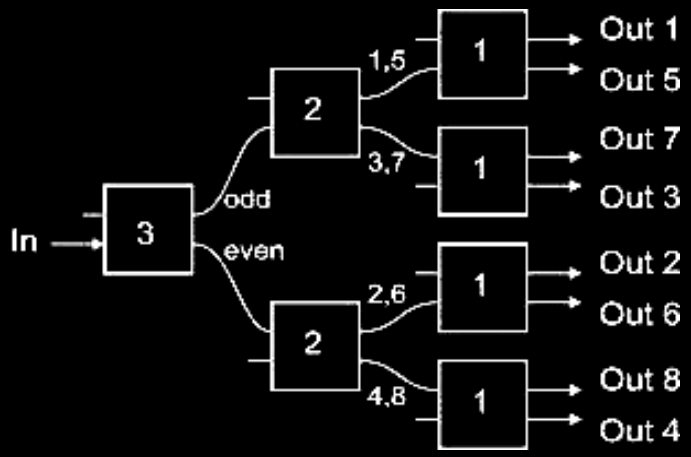
[S.Assefa et al, OE, April 2010]
[B.Lee et al, OFC 2010, PDP]

http://www.research.ibm.com/photonics

Nanophotonics components: WDM multiplexer

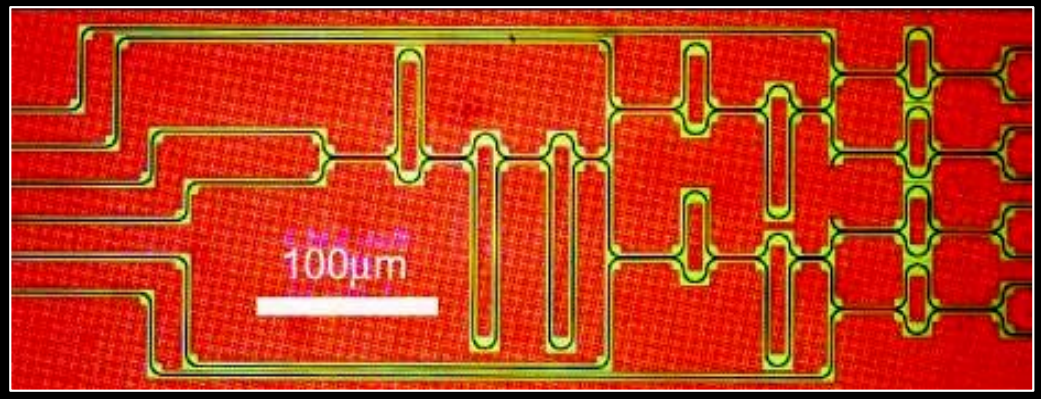
Cascaded Mach-Zehnder WDM filter

Design



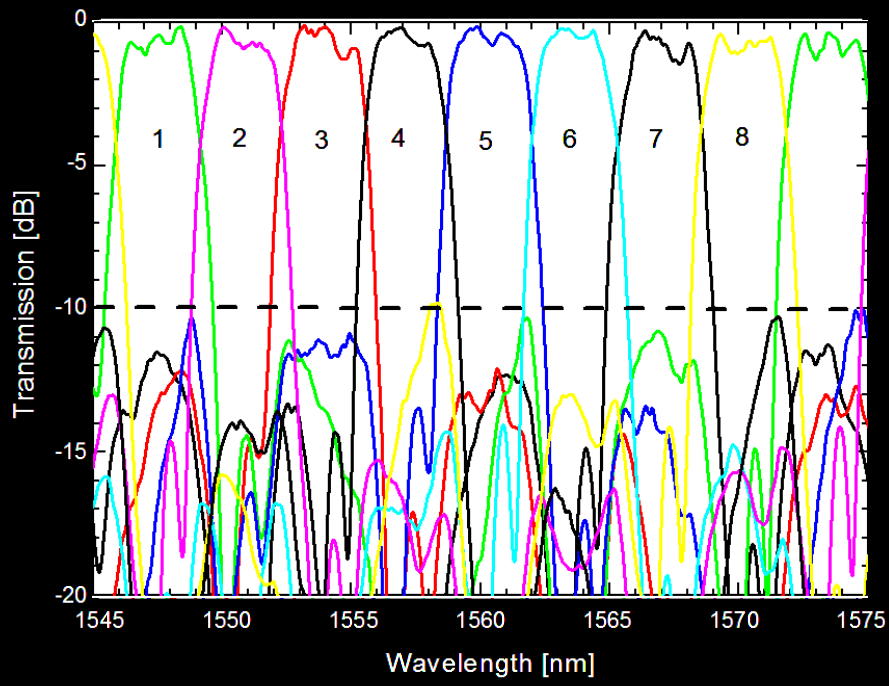
- 3-stage MZI
- 8 outputs
- 3.2nm spacing
- 2nm flat-top

Die photo



✓Footprint 360 x 170 µm
✓65nm design rules provide control of critical dimensions
✓No active tuning required

Performance



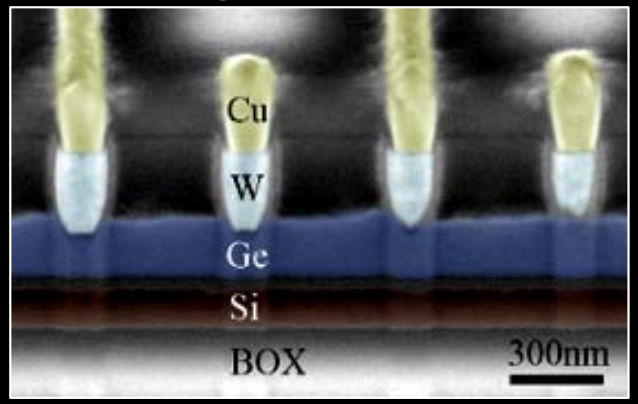
✓ WDM integrated with CMOS Circuitry
✓ 8 channels; 3.2nm spacing
✓ 2nm flat-top response; 1dB in-band ripple
✓ Better than -10dB cross-talk
✓ Temperature tolerant within ±10°C

[F.Horst et al, OFC 2010, Invited talk]
[F.Horst et al, PTL, 21 (2009)]

http://www.research.ibm.com/photonics

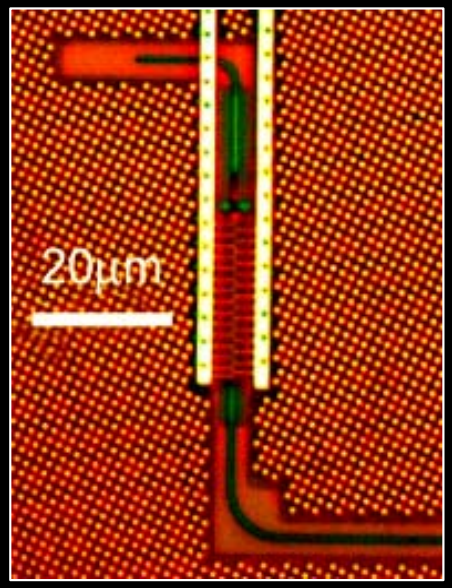
Nanophotonics components: Detectors

Design

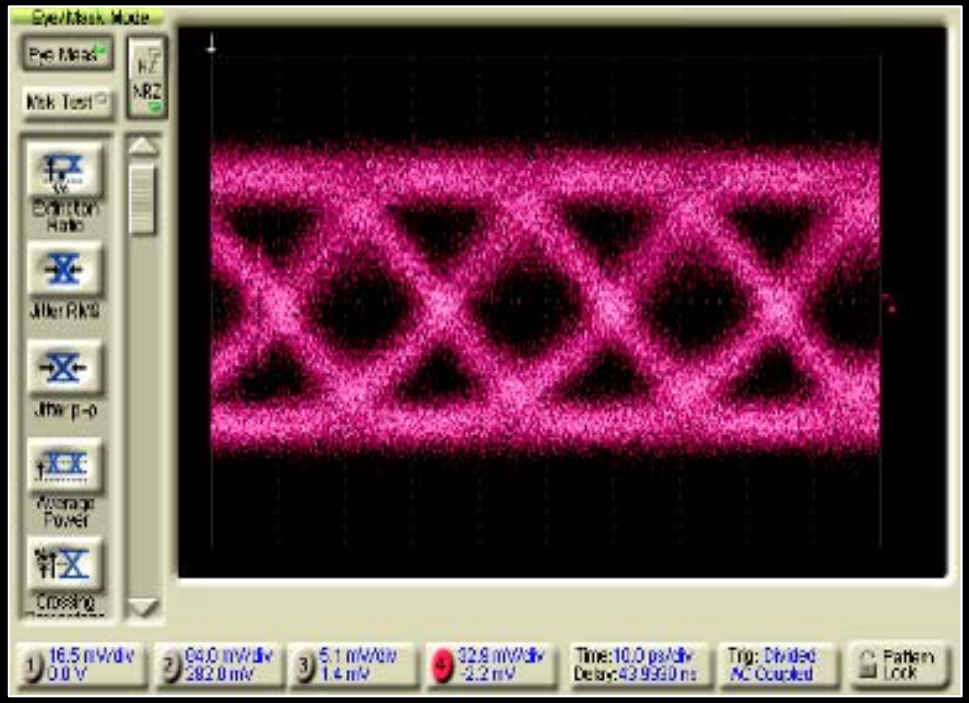


- Ge-first prior to SD anneal
- Standard CMOS metallization
- MSM junction to Ge-on-Insulator

Die photo



Performance



40Gbps open eye at 2V bias

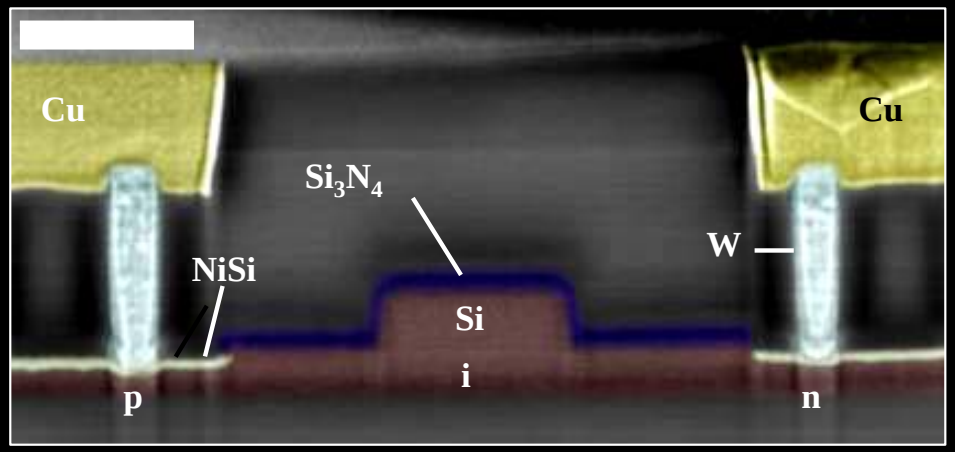
- ✓Ge detector integrated with CMOS Circuitry
- ✓Avalanche gain 10dB with only 1.5V bias
- ✓40GHz bandwidth with CMOS bias voltages

[S.Assefa et al, Nature, March 2010]
[S.Assefa et al, OE, April 2010]

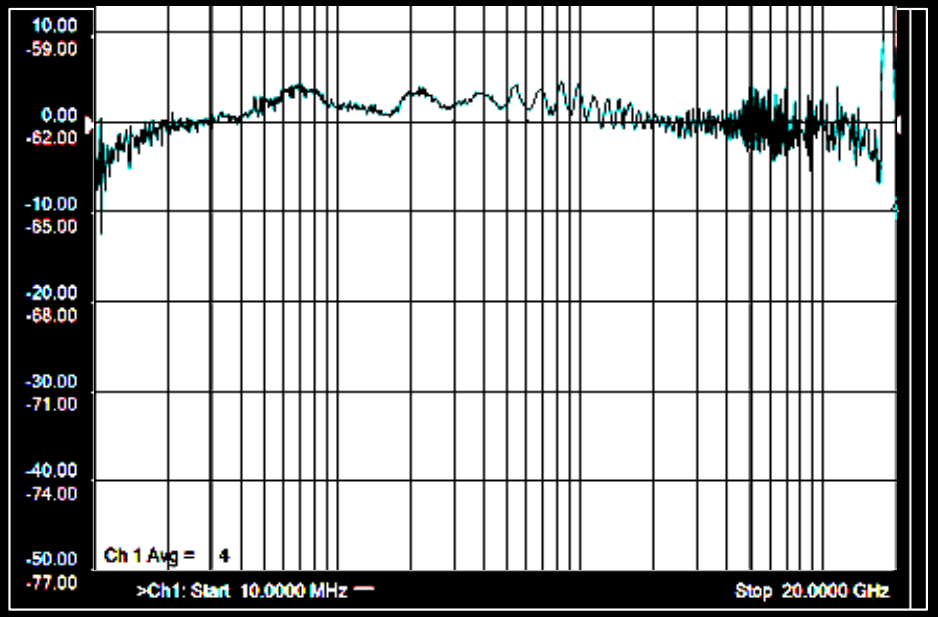
http://www.research.ibm.com/photonics

Nanophotonics components: Modulators

Design

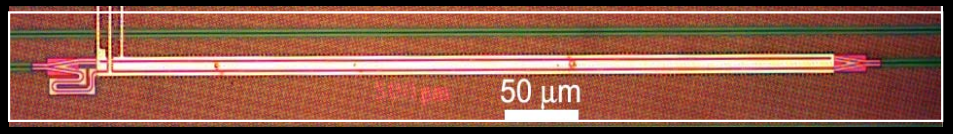


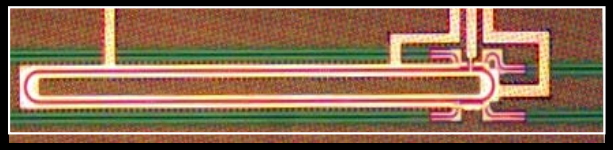
Performance



Over 20GHz modulation bandwidth

Die photo





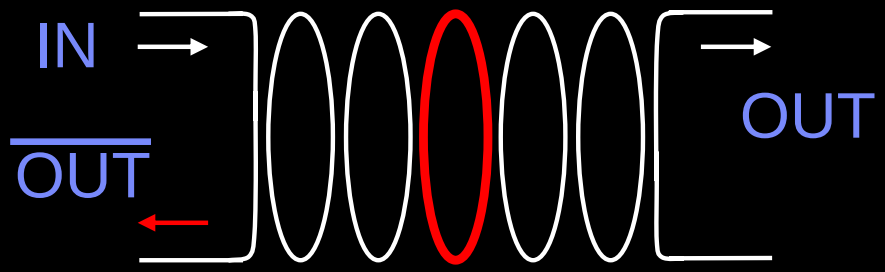
- ✓ Modulator integrated with CMOS Circuitry
- ✓ Library of forward and reverse biased devices
- ✓ Over 10Gbps modulation bandwidth

[W.Green et al, OE, 2007]
[J. Van Campenhout et al, OE, December 2010]

http://www.research.ibm.com/photonics

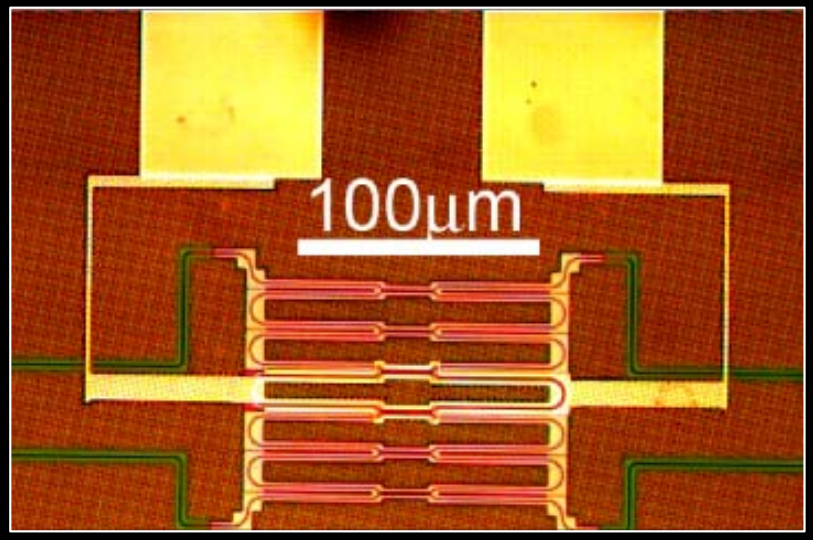
Nanophotonics components: Switches

Design

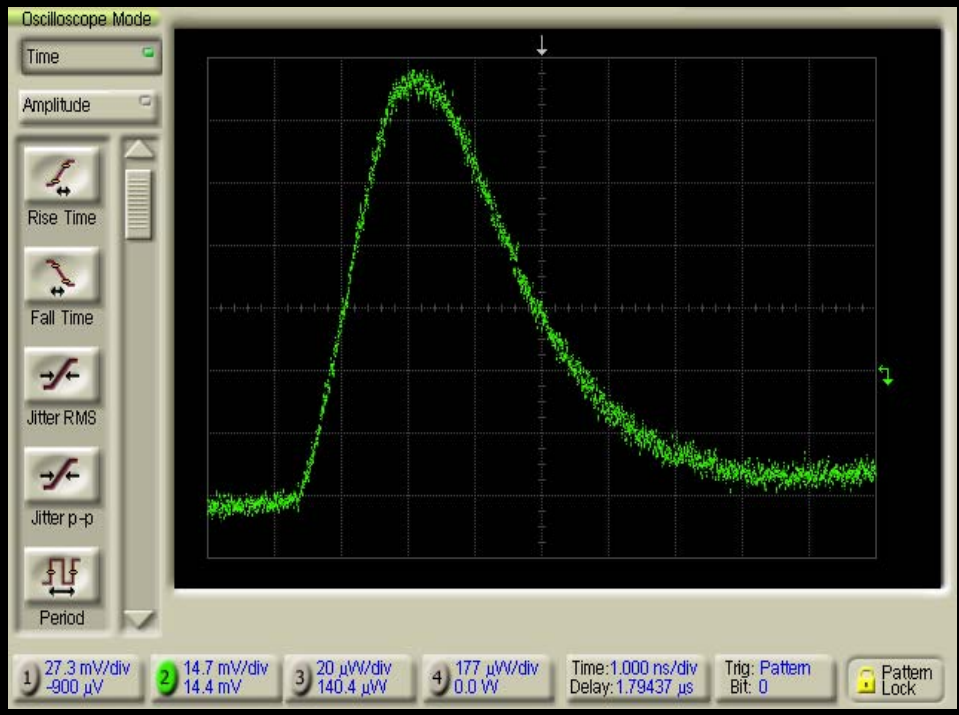


- 5-stage ring resonator design
- Central ring with PIN diode
- 2x2 electro-optical switch

Die photo



Performance



5ns switching time

✓Optical switch integrated with CMOS Circuitry
✓5ns switching time

[Y.Vlasov et al, Nature Phot., April 2008]
[J. Van Campenhout et al, OE, April 2009]
[J. Van Campenhout et al, CLEO 2010]

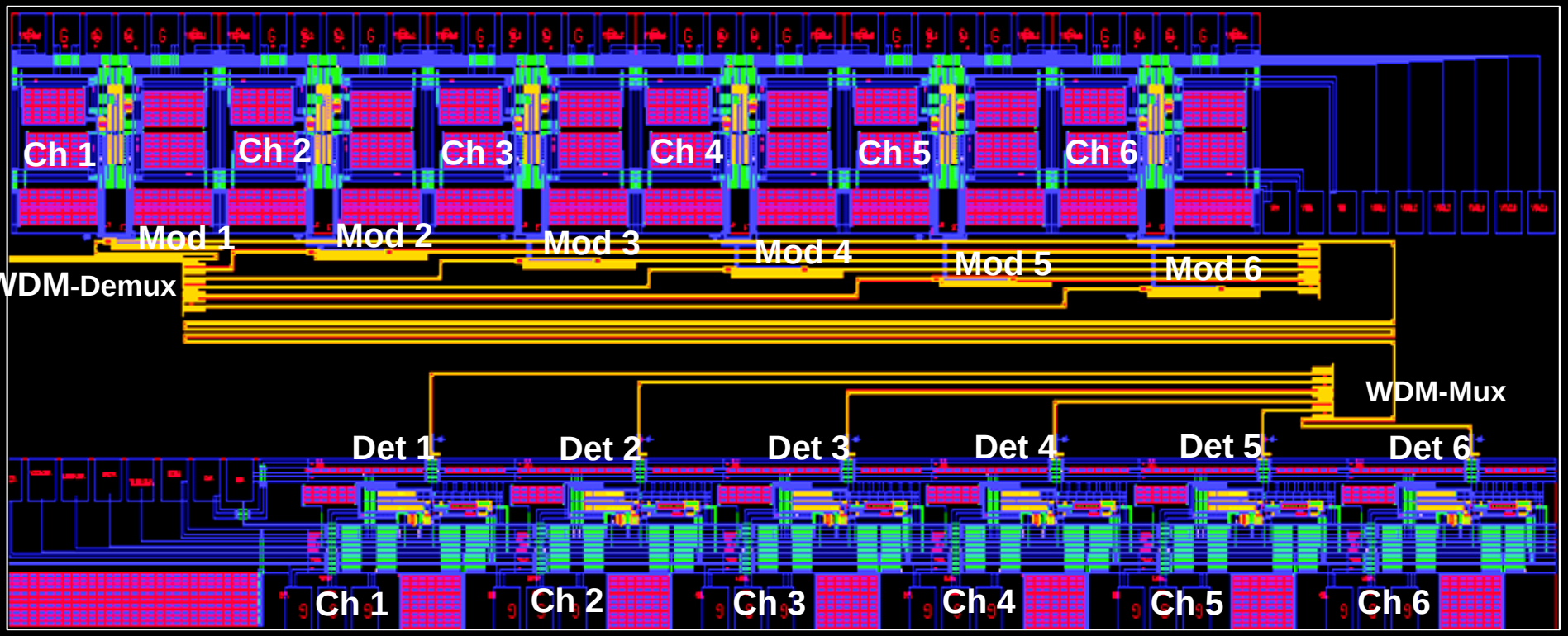
http://www.research.ibm.com/photonics

SNIPER project at IBM Research

- Design and Layout
  (Nanophotonics and CMOS together)

Co-design and Co-layout of CMOS and Nanophotonics components

- Library of Nanophotonics components
- Photonics-enabled design rules
- Photonics-enabled DRC



Layout snapshot

✓Allows to layout complex CMOS and Nanophotonics circuits

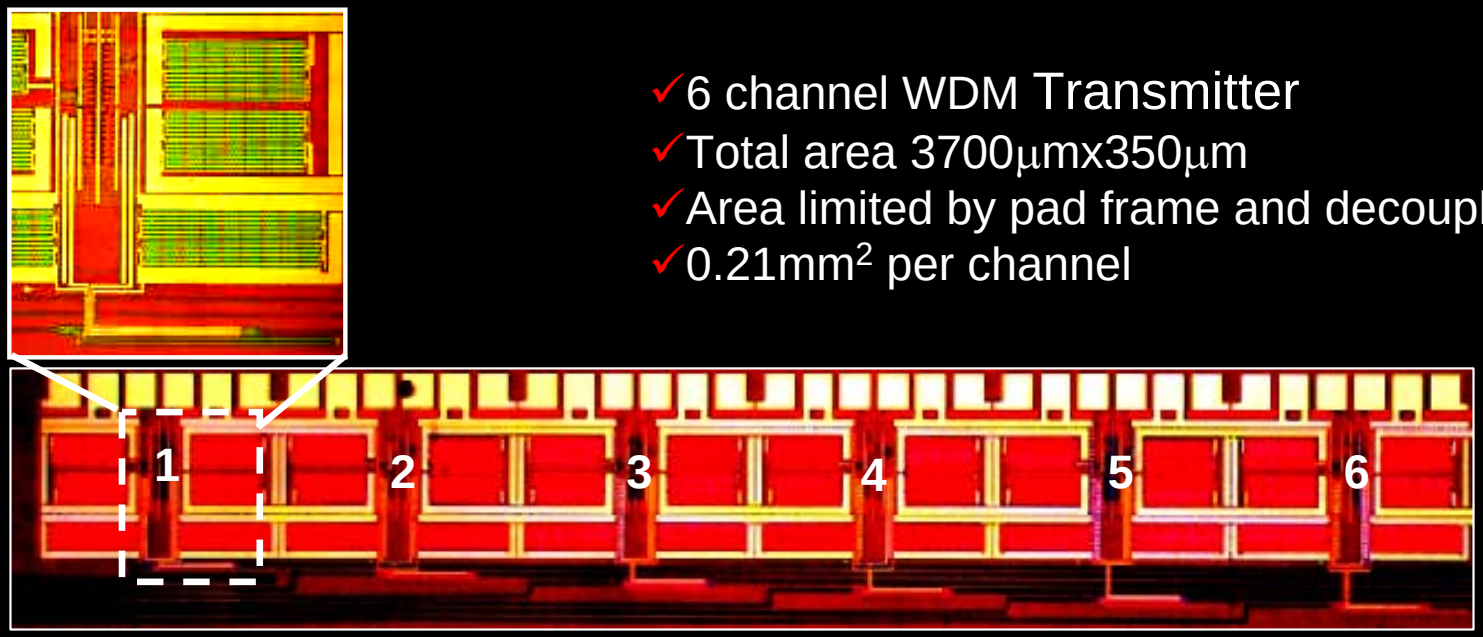
http://www.research.ibm.com/photonics

SNIPER project at IBM Research

- Integration density

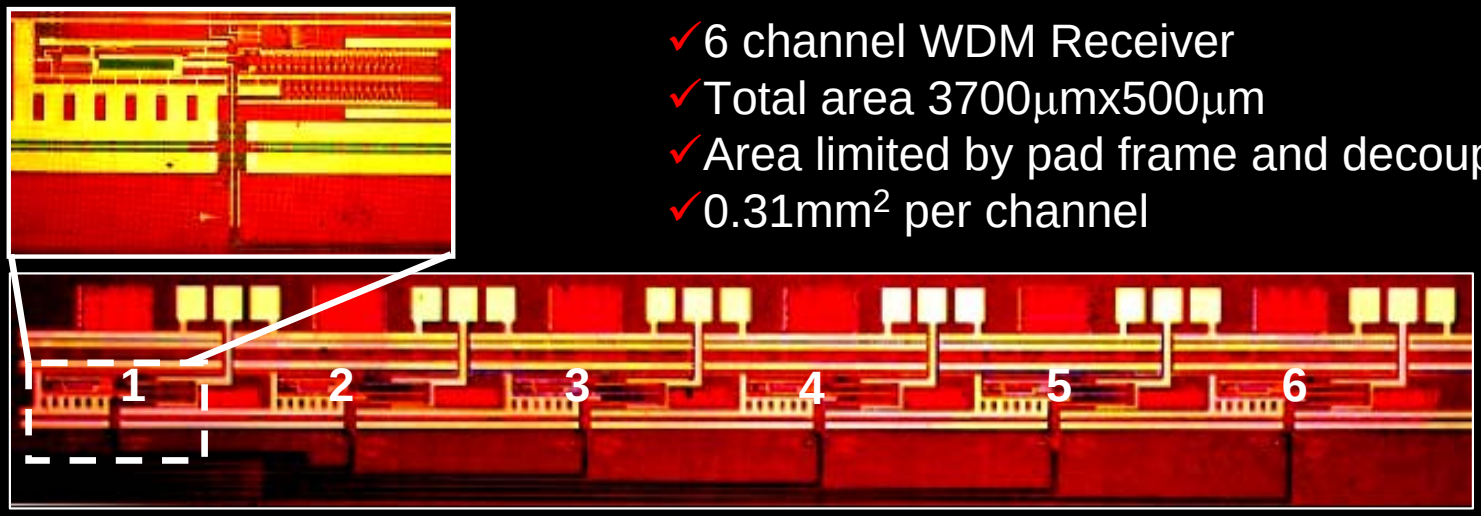
Integrated CMOS and Nanophotonics modules

Transmitter: 6 WDM channels



- ✓6 channel WDM Transmitter
- ✓Total area 3700μmx350μm
- ✓Area limited by pad frame and decoupling capacitors
- ✓0.21mm^2 per channel

Receiver: 6 WDM channels



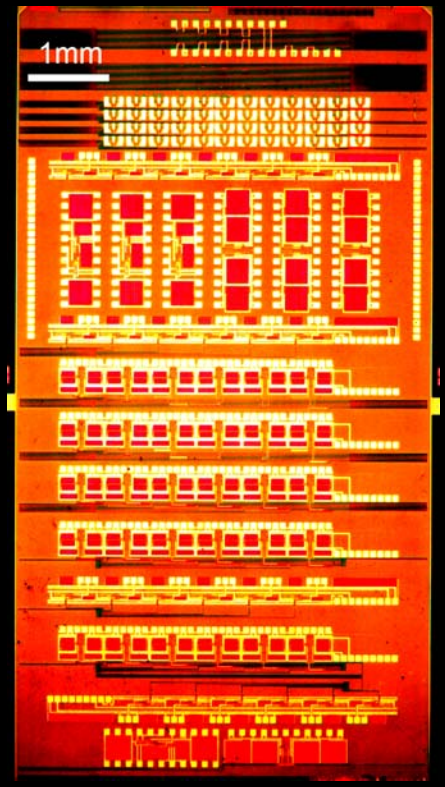
- ✓6 channel WDM Receiver
- ✓Total area 3700μmx500μm
- ✓Area limited by pad frame and decoupling capacitors
- ✓0.31mm^2 per channel

Comparison of IBM CMOS Nanophotonics with existing Si Photonics

Si CMOS Photonics

Others (Announced)

- ✓ 130nm design rules for CMOS
- ✓ 130nm design rules for Micro-Photonics
- ✓ CMOS FEOL integrated (Ge-last after activation)
- ✓ Large Litho variations - active tuning is required
- ✓ 6mm^2 per transceiver channel



Si CMOS Nano-Photonics

IBM (Announcing now)

- ✓ 130nm design rules for CMOS
- ✓ 65nm design rules for Nano-Photonics
- ✓ CMOS FEOL integrated (Ge-first prior to activation)
- ✓ Small Litho variations - active tuning not required
- ✓ 0.5mm^2 per transceiver channel

IBM CMOS Nanophotonics technology:

- ➢ 10x higher integration density
- ➢ The only amenable for Terabit/s-class single-chip CMOS transceivers
- ➢ 50channels x 20Gbps = 1Tbps transceiver occupies only 5x5mm^2 of a CMOS die (can be smaller than 2x2mm^2 without pad frame and capacitors)

http://www.research.ibm.com/photonics

Conclusions

- IBM has developed technology for monolithic integration of Nanophotonics WDM transceivers into the standard CMOS front-end
- IBM technology shows 10X improvement in integration density
- Enables low power Tbps-class CMOS transceivers for future Exascale systems
- Pursue integration into deeply scaled IBM CMOS processes

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